2811

PATENT
Attorney Docket No.: SAM-0260

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s): Jung-Lim Yoon, et al.
Serial No.: 09/974,025
Filing Date: October 10, 2001
Title: FLIP CHIP TYPE SEMICONDUCTOR DEVICE AND METHOD OF FABRICATING THE SAME

Examiner: Parekh, N.
Group Art Unit: 2811

CERTIFICATE OF MAILING UNDER 37 C.F.R. § 1.8

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6-12-03
Date

Amy Green

Mail Stop Non-Fee Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

TRANSMITTAL LETTER

Sir:

Enclosed herewith for filing in the above-identified patent application please find the following listed items:

1. ~~Response in response to Office Action mailed on March 13, 2003; and~~
2. Return Postcard.

In connection with the foregoing matter, please charge any additional fees which may be due, or credit any overpayment, to Deposit Account Number 50-1798. A duplicate copy of this letter is provided for this purpose.

Respectfully submitted,

Date: June 12, 2003

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6/10/03

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#1 Response Initialed 6/20/03

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RESPONSE

Sir:

This is in response to the Office Action mailed on March 13, 2003.

Claims 1 and 3-5 are rejected under 35 U.S.C. §102(e) as being anticipated by Greer (U.S. Patent Number 6,451,681). Claim 2 is rejected under 35 U.S.C. §103(a) as being unpatentable over Greer in view of the admitted prior art (APA). In view of the following remarks, the applicants respectfully traverse the rejections and request reconsideration.

In the applicants' invention, a flip chip semiconductor device has pad and fuse areas. An interlayer insulation layer is formed on a semiconductor substrate, and a passivation layer is formed on the interlayer insulation layer. A first metal line is formed in a first region of the passivation layer in the pad area, and a pair of second metal lines is formed in a region of the passivation layer in the fuse area. A pad covers a portion of the first metal line in the pad area, and a fuse covers the pair of second metal lines and the passivation layer therebetween in the fuse area. A polyimide layer covers the surface of the semiconductor substrate including the pad and

the fuse, and the polyimide layer has a pad opening that exposes the pad. An under-bump metal layer pattern and a bump are formed on the exposed pad in the polyimide layer.

The applicants' claims specifically set forth the features of the invention. For example, the claims specifically set forth that the first metal line in the pad area is formed in the passivation layer and also that the second metal lines in the fuse area are also formed in the passivation layer. Because the metal lines are formed in the passivation layer, instead of the interlayer insulation layer (interlayer dielectric ILD), the passivation layer need not be patterned to accommodate the pad and fuse overlying the metal lines.

In Greer, a first level interconnect 120 is formed in a second interlevel dielectric (ILD) layer 118. An interconnect 126, including an adhesion/barrier film 122 and a copper fill material 124, is then formed over the first level interconnect 120, also within the second ILD layer 118. In the embodiment disclosed in Greer in connection with Figure 3, a passivation layer 300 is then formed over the interconnect 126. Likewise, in the embodiments of Figures 7 and 8, a passivation layer 704 is formed over the interconnect 126. In the embodiment of Figure 3, the passivation layer 300 is then patterned to allow for a transitional metallurgy 312 to be formed over the interconnect 126 and the under-bump layer 314 and bump 310 to be formed over the transitional metallurgy 312. In the embodiment of Figures 7 and 8, the passivation layer 704 is patterned to accommodate the fuse structure 710 and the transitional metallurgy 806, respectively. Thus, the interconnects 126 are not formed in the passivation layers in Greer, as specifically claimed by the applicants.

The Examiner refers to layer 118 in Greer as a insulating dielectric/passivation layer. The applicants respectfully disagree with the Examiner's assessment of what is taught by the reference. Referring to Greer at column 3 line 12, layer 118 is a second ILD formed over a first ILD 116 and the first level interconnect 120. Layer 118 is not a passivation film. Furthermore, Greer specifically teaches at column 4 line 25 that layer 300 in Figure 3 is a passivation layer and at column 7 line 31 that layer 704 is a passivation layer. Hence, the passivation layer in Greer is formed over the interconnect 126, and the interconnect 126 is formed in an ILD film.

Hence, the Greer reference fails to teach or suggest the invention claimed by the applicants. That is, specifically, Greer fails to teach or suggest the applicants' first and second metal lines formed in regions of a passivation layer, a pad covering a portion of the first metal line and a fuse covering the second metal lines and the passivation layer therebetween. The Examiner refers to the conductive material 124 in Greer as the applicants' claimed first and second metal lines. However, item 124 is not formed in a passivation layer. Since Greer fails to teach or suggest the invention set forth in the claims, it is believed that the claims are allowable over Greer, and reconsideration of the rejections of claims 1 and 3-5 under 35 U.S.C. §102(e) based on Greer is respectfully requested.

Regarding the rejection of claim 2, Figure 1 of the present application, like Greer, shows metal lines 10a and 10b formed in an interlayer insulation layer 5, not a passivation layer. The passivation layer 18 shown in Figure 1, again, as in Greer, is formed over the metal lines and interlayer insulation layer in which the metal lines are formed. Accordingly, Figure 1 of the application also fails to teach or suggest the invention claimed by the applicants. That is, Figure 1 fails to teach or suggest first and second metal lines formed in a passivation layer, a pad covering a portion of the first metal line and fuse covering the second metal line and the passivation layer therebetween. As noted above, Greer also fails to teach or suggest these claimed features of the invention. Accordingly, no combination of the references would result in providing such teaching or suggestion. Therefore, it is believed that claim 2 is allowable over the combination of Greer and the APA, and reconsideration of the rejection of claim 2 under 35 U.S.C. §103(a) as being unpatentable over Greer in view of the APA is respectfully requested.

In view of the foregoing remarks, it is believed that all claims pending in the application are in condition for allowance, and such allowance is respectfully solicited. If a telephone conference will expedite prosecution of the application, the Examiner is invited to telephone the undersigned.

Respectfully submitted,

Date: June 12, 2003

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